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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/670,497

09/26/2003

Paul A. Farrar

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
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EXAMINER

VU, DAVID

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/670,497

Applicant(s)

FARRAR, PAUL A.

Examiner

DAVID VU

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 76-83 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 76-83 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>09/26/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 76-80, 82 and 83 are rejected under 35 U. S. C. 103(a) as being anticipated by Hasegawa et al. (US Pat. 6,593,246, herein after Hasegawa).

Regarding claim 76, Hasegawa discloses an integrated circuit structure, comprising:
a SILK insulating layer 13 having a thickness of 300-800nm (3,000-8,000Å) (col. 6, lines 8-25 and col. 12, lines 9-12) provided over a semiconductor substrate 11 and contacting at least a portion of a metal layer 53 provided within semiconductor substrate 11; a 400nm (4,000Å) NANOGLOSS insulating layer 14 (col. 8, lines 24-30; col. 7, lines 29-32) provided over SILK insulating layer 13; and a first opening within SILK and NANOGLOSS insulating layers (fig. 3F). According to the present Specification, page 11, lines 17-20, both the SILK and NANOGLOSS layers ($k_{\text{SILK}} = 2.56$ and $k_{\text{NANOGLOSS}} = 3.5$ at 100kHz) have a dielectric constant lower than 4.0.

Hasegawa discloses a 400nm (4,000Å) NANOGLOSS insulating layer 14 (col. 8, lines 24-30; col. 7, lines 29-32) but fails to disclose a NANOGLOSS insulating layer having a

thickness of 100-2,000Å. It would have been obvious to one with ordinary skill in the art at the time of the invention for forming a NANOGLOSS insulating layer having a thickness as taught by Hasegawa. Although the Hasegawa range is higher than the claimed range, this does not define patentable over Hasegawa since the thickness of an insulating layer is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art. The specific thickness of an insulating layer does not provide any critical or unexpected results to an integrated circuit structure. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

Regarding claim 77, Hasegawa discloses that the first and second dielectric (13/14) can be "repeated" such that a third and fourth insulating layers with a dielectric constant lower than 4.0 are necessarily provided over NANOGLOSS insulating layer 14; and a second opening within third and fourth insulating layers (col. 10, lines 20-26).

Regarding the limitation that the opening being formed by time etching of at least one of SILK and NANOGLOSS insulating layers with an etch chemistry (claims 76 and 77), such limitation does not further define the structure as instantly claimed, nor serve to distinguish over Hasegawa. Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173

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USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw make clear.

Regarding claim 78, Hasegawa discloses third and fourth insulating layers are formed of different materials which can be selectively etched relative to each other (col. 10, lines 20-26 and col. 9, lines 43-47).

Regarding claim 79, Hasegawa discloses third and fourth insulating layers comprise organic material (col. 6, lines 18-25 & 37-39 and col. 7, line 33 through col. 8, line 24).

Regarding claim 80, Hasegawa discloses organic material is selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene and SILK (col. 6, lines 18-25; lines 37-39 and col. 7, line 33 through col. 8, line 24). According to the present Specification, page 11, lines 17-20, $k_{\text{SILK}} = 2.56$ at 100kHz.

Regarding claim 82, Hasegawa discloses third and fourth insulating layers comprise inorganic material (col. 6, lines 29-35 and col. 8, lines 24-30).

Regarding claim 83, Hasegawa discloses inorganic material is selected from the group consisting of NANOGLASS (col. 8, lines 24-30). According to the present Specification, page 11, lines 17-20, $k_{\text{NANOGLASS}} = 3.5$ at 100kHz.

2. Claim 81 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Hasegawa et al. (US Pat. 6,593,246) in view of Baklanov et al. (US Pat. 6,593,251, herein after Baklanov).

Hasegawa does not disclose fourth insulating layer comprises organic SILK material and third insulating layer comprises inorganic NANOGLASS material but rather that the third and fourth insulating layers are generally organic 13/inorganic 14 (col. 6, lines 18-25 & 37-39 and col. 8, lines 24-30) or inorganic/organic (col. 4, line 65 through col. 5, line 2) respectively.

Baklanov discloses that NANOGLASS is a suitable inorganic dielectric (col. 3, line 20) and SILK is a suitable organic dielectric (col. 3, lines 16-17) for the Inter-Layer Dielectric applications described by Hasegawa. It would have been obvious to one of ordinary skill in the art at the time the invention was made to chose NANOGLASS and SILK as the third (inorganic) and fourth (organic) insulating layers in Hasegawa device because these materials have a low dielectric constant and have the properties required by the teaching of Hasegawa. The motivation for specifically picking NANOGLASS and SILK as the inorganic and organic dielectric layer is that such materials have a low dielectric constant such that parasitic capacitance between conductors is reduced.

Response to Arguments

3. Applicant's arguments with respect to claims 76-83 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can

be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David Vu

November 10, 2004



David Nelms
Supervisory Patent Examiner
Technology Center 2800